Application Note
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MAJIC® Interface Specifications for MIPS EJTAG

0380-0181-10 Rev 2.2

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Introduction

This application note provides technical specifications for the MAJIC® Series of Intelligent Debug Probes when used with processors that support the MIPS EJTAG debug interface.

- Cabling options.
- Debug connector details: pin-outs and recommended part numbers.
- Board design considerations.
- Electrical specifications for each model in the MAJIC® Series of Intelligent Debug Probes.

Cable Kit Options

There are several cable kit options available for the MAJIC® Series, and it is important to choose the right cable kit(s) for your target board(s) and MAJIC® model. The following table shows the most commonly used cable kits for target boards incorporating a MIPS processor with an EJTAG debug interface. Details on the connectors' pin-outs, and recommended board design practices follow on the next few pages.

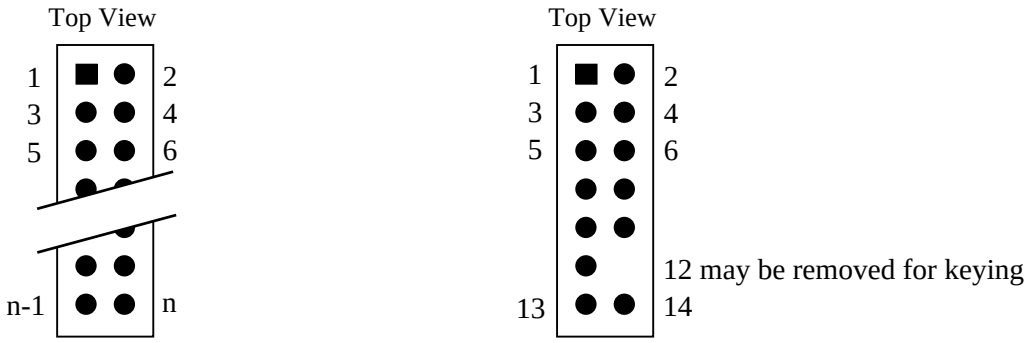
Target Connector	**MAJIC (I, II, or III) MAJIC^{MX} (I, II) MAJICO**	**MAJIC^{PLUS}**	**MAJIC^{PLUS}/II**
10-Pin 0.1" IEEE standard JTAG	CK-J10	CKP-J10	CKP2-J10
12-Pin 0.1" IEEE standard JTAG plus RST*	CK-J12	CKP-J12	CKP2-J12
14-Pin 0.1" EJTAG v2.5 (and later), no trace	CK-MIPS14	CKP-MIPS14	CKP2-MIPS14
12-Pin 0.05" EJTAG v2.0, no trace	CK-EJ12	CKP-EJ12	CKP2-EJ12
20-Pin 0.05" EJTAG v2.0 (3 PCST, 1 TPC)	CK-EJ20	CKP-EJ20	AP2-EJ20
24-Pin 0.05" IDT RC323xx (3 PCST, 1 TPC)	CK-IDT24	CKP-IDT24	AP2-IDT24
28-Pin 0.05" EJTAG v2.0 (6 PCST, 2 TPC)	CK-EJ28	CKP-EJ28	AP2-EJ28
38-Pin 0.05" EJTAG v2.0 (6 PCST, 4 TPC)	CK-EJ38	CKP-EJ38	AP2-EJ38
52-Pin 0.05" EJTAG v2.0 (12 PCST, 8 TPC)	CK-EJ52	CKP-EJ52	AP2-EJ52

Notes: The connectors listed above are the most common, but EPI supports many others as well. If the connector you have is not listed, please contact EPI for more information.

If you are trying to decide which connector to use on your own hardware design, and do not need PCTrace, then EPI recommends either the MIPS14 for ease of use, or the EJ12 for small form factor applications. If you do want to support PCTrace on your board, then you must choose the EJxx with the right pin-out (see table below), or IDT24 for RC323xx based designs.

JTAG Headers

- EJTAG specification v1.5.3 and v2.0 call for dual row male headers with 0.05”x0.05”spacing. The number of pins that are required depends on the PCTrace capability of the particular processor in use. EPI recommends using the Samtec FTSH-1xx-01-F-DV-A connector series.
- EJTAG v2.5 and later calls for a 14-pin dual row male header with 0.1”x0.1” spacing. EPI recommends using 3M part number 2414-600UB.



Note: The debug connector pin-outs and recommended connection is shown in the following table. Additional technical details on the JTAG signals are discussed in the *Board Design Considerations* and *Electrical Specifications* sections of this application note.

Pin-out and Connection Notes

Pin	CK/CKP_EJxx		CK/CKP_IDT24	
1	TRST* **-or-** TPC (Note)	10k pull-up 33 Ω series	TRST*	10k pull-up
3	TDI/DINT*	10k pull-up	TDI/DINT*	10k pull-up
5	TDO/TPC	33 Ω series	TDO/TPC	33 Ω series
7	TMS	10k pull-up	TMS	10k pull-up
9	TCK	10k pull-up	TCK	10k pull-up
11	RST*	10k pull-up	RST*	10k pull-up
13	PCST[0]	33 Ω series	PCST[0]	33 Ω series
15	PCST[1]	33 Ω series	PCST[1]	33 Ω series
17	PCST[2]	33 Ω series	PCST[2]	33 Ω series
19	DCLK	33 Ω series	DCLK	33 Ω series
21	TPC[2]	33 Ω series	DebugBoot	10k pull-down
23	PCST2[0]	33 Ω series	VIO	10k pull-up
25	PCST2[1]	33 Ω series		
27	PCST2[2]	33 Ω series		
29	TPC[3]	33 Ω series		
31	PCST3[0]	33 Ω series		
33	PCST3[1]	33 Ω series		
35	PCST3[2]	33 Ω series		
37	TPC[4]	33 Ω series		
39	PCST4[0]	33 Ω series		
41	PCST4[1]	33 Ω series		
43	PCST4[2]	33 Ω series		
45	TPC[5]	33 Ω series		
47	TPC[6]	33 Ω series		
49	TPC[7]	33 Ω series		
51	TPC[8]	33 Ω series		
All even numbered pins should be flashed to the ground plane.				

Pin	CK/CKP_MIPS14	
1	TRST*	10k pull-up
2	GND	
3	TDI	10k pull-up
4	GND	
5	TDO	33 Ω series
6	GND	
7	TMS	10k pull-up
8	GND	
9	TCK	10k pull-up
10	GND	
11	RST*	10k pull-up
12	Key	(no pin)
13	DINT	10k pull-down
14	VIO	10k pull-up

Board Design Considerations

This section provides additional information on board design considerations that arise when designing a target board which incorporates a MIPS processor with EJTAG debug interface.

Reset Management

- The RST* signal should be connected so that the target system (including the CPU) will be reset when it is asserted (low) by the MAJIC® probe, but will not result in TRST* (JTAG reset) being asserted on the target processor. This allows the MAJIC® probe to reset the target system upon command from the user. When both cold and warm resets are provided, warm reset is recommended. This is an optional feature, but RST* should be pulled up to the target's I/O voltage regardless of whether the reset feature is implemented.
- The nSRST signal is an open-collector signal, so you must provide a pull-up for this signal. It may be tied directly to the reset switch or power-up reset circuit on your board.

JTAG Interface

- The TRST* signal connection to the processor is optional, but it is recommended that the connector pin be pulled up irrespective of whether it is connected to the processor. It is acceptable to pull down the TRST* pin, providing that you configure the MAJIC® probe to enable its TRST* output driver.
- Some CPU data sheets recommend a pull-down on certain JTAG signals instead of a pull-up. The MAJIC® probe can support that recommendation, but the signals should not be left floating.
- Some processors can replace TRST* with a demultiplexed TPC so the processor may be daisy chained with other JTAG devices. In this case a 33 Ω series termination resistor should be placed as close as possible to the respective processor pin and no pull-up should be used.

PCB Layout

- Avoid placing any tall components near the EJTAG connector, and locate it in a way that is easy to reach (near the edge of the board). We recommend clearly labeling the EJTAG connector and the position of pin 1 on the PCB.
- If you have more than one JTAG device on the scan chain, then the debug connector should be at the end of the JTAG nets, not in the center of the nets (i.e. the JTAG signals must not fan out from the debug connector to multiple devices). Please refer to the *MAJIC® Support for Multi-TAP JTAG Configurations* application note (P/N 0380-0243-10) for additional information, especially if your target supports PCTrace.
- It is important to keep the PCTrace DCLK, TDO/TPC, TPC*n*, and PCST*n* signals short, and even more important to make them equal in length. The 33 Ω series termination resistors placed as close as possible to their respective processor pins. If the trace pins can be reconfigured for alternate signals, you should provide a build option to disconnect their alternate function.
- All unused PCTrace pins should be grounded or pulled up.

Electrical Characteristics

This section provides the JTAG and PCTrace electrical characteristics for each model in the MAJIC® Series of Intelligent Debug Probes.

JTAG Interface for MAJIC®/I Series

DC Characteristics	Note	Specification
Target I/O Voltage		1.65V (1.8V nominal) to 3.5V CMOS 3.3V or 5V TTL
Output Drive: TCK		± 6mA at 1.8V ± 12mA at 2.5V ± 18mA at 3.3V
Output Drive: TRST*, TMS, TDI		± 4mA at 1.8V ± 6mA at 2.5V ± 8mA at 3.3V
Output Drive: RST*	1.1	+3mA/-40µA at 1.8V +8mA/-70µA at 2.5V +16mA/-90µA at 3.3V
Input Loading: TDO		20pF to ground 10k pull-up to I/O voltage
AC Characteristics		
TCK Frequency		<1 - 40MHz (programmable)
TCK Duty Cycle		40/60% to 60/40%
Target Setup Requirement: TMS, TDI to TCK↑	1.2, 1.4	5ns max at 1.8V
Target Hold Requirement: TMS, TDI after TCK↑	1.2, 1.4	5ns max at 1.8V
Target Output Delay: TCK↓ to TDO	1.3, 1.4	0ns min, 7ns max, at 1.8V

Notes:

1.1: RST* is a pseudo-open-collector output, with a 10k pull-up to the I/O voltage level.

1.2: Targets requiring greater setup or hold times on their TMS/TDI inputs may be accommodated by reducing the MAJIC® probe's JTAG interface clock frequency.

1.3: Targets with a slower TDO driver may be accommodated by reducing the MAJIC® probe's JTAG interface clock frequency.

1.4: At higher I/O voltages, the MAJIC® probe's JTAG timing improves and target JTAG requirements are less stringent.

JTAG Interface for MAJIC®/II Series

DC Characteristics	Note	Specification
Target I/O Voltage		1.2v to 3.3v (nominal)
Output Drive: TCK, TRST*, TMS, TDI		± 2mA at 1.2v ± 6mA at 1.8V ± 18mA at 2.5V ± 24mA at 3.3V
Output Drive: RST*	2.1	+2mA at 1.2v, -120µA at 1.2v +6mA, -180µA at 1.8v +8mA, -250µA at 2.5v +16mA, -330µA at 3.3v
Input Loading: TDO		45pF to ground 10k pull-up to I/O voltage
AC Characteristics		
Max TCK Frequency (75pF load)	2.2	40MHz at 3.3v 20MHz at 1.8v 10MHz at 1.2v
TCK Duty Cycle		40/60% to 60/40%
Target Setup Requirement: TMS, TDI to TCK↑	2.3	4ns max at 3.3v 40MHz
Target Hold Requirement: TMS, TDI after TCK↑	2.3	5ns max at 3.3v 40MHz
Target Output Delay: TCK↓ to TDO	2.4	0ns min, 5ns max, at 3.3v

Notes:

2.1: RST* is a pseudo-open-collector output, with a 10k pull-up to the I/O voltage level.

2.2: Maximum frequency is a function of the I/O voltage level vs. capacitive loading. Therefore, the maximum supported frequency may be constrained on low voltage targets, and targets with heavily loaded JTAG pins. The MAJIC® probe's TCK frequency is programmable, from <1 to 40MHz.

2.3: Targets requiring greater setup or hold times on their TMS/TDI inputs may be accommodated by reducing the MAJIC® probe's JTAG interface clock frequency.

2.4: Targets with a slower TDO driver may be accommodated by reducing the JTAG interface clock frequency.

JTAG Interface for MAJIC®/III and MAJICO™

DC Characteristics	Note	Specification
Target I/O Voltage		3.3v (nominal)
Output Drive: TCK, TRST*, TMS, TDI		± 4mA
Output Drive: RST*	3.1	+1.5mA, -3μA
Input Loading: TDO		30pF to ground 10k pull-up to I/O voltage
AC Characteristics		
TCK Frequency		10MHz
TCK Duty Cycle		40/60% to 60/40%
Target Setup Requirement: TMS, TDI to TCK↑		13ns (max)
Target Hold Requirement: TMS, TDI after TCK↑		26ns (max)
Target Output Delay: TCK↓ to TDO		0ns (min) 86ns (max)

Note:

3.1: RST* is a pseudo-open-collector output, with a 10k pull-up to the I/O voltage level.

MAJIC$^{PLUS®}$/I PCTrace Specifications

PCTrace interface requirements for a MAJIC$^{PLUS®}$/I with a CKP-EJxx passive probe.

DC Characteristics	Note	Specification
Target I/O Voltage		2.8V (3.0V nominal) to 3.5V CMOS 3.3V or 5V TTL
TDO/TPC signal		20pF to ground 10k pull-up to I/O voltage
Input Loading: DCLK	4.1	20pF to ground 1k pull-up to I/O voltage
Input Loading: TPC*n*, PCST*n*		30pF to ground 10k pull-up to I/O voltage
AC Characteristics		
DCLK Frequency		DC - 100MHz
High Time: DCLK		4ns min
Low Time: DCLK		4ns min
MAJIC® Setup Requirement: TPC*n*, PCST*n* to DCLK↓		0ns min
MAJIC® Hold Requirement: TPC*n*, PCST*n* after from DCLK↓		4ns min

Note:

4.1: Targets must be capable of driving at least ± 4mA for DCLK; a stronger driver (such as ± 8mA) is recommended. The target's DCLK drive capability is critical when attempting to capture trace data near the maximum frequency rating.